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11-14-05

PATENT APPLICATION

ATTORNEY DOCKET NO. 10971353-3

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): David P. Hannum et al.

Confirmation No.: 1941

Application No.: 10/687,907

Examiner: D. Tran

Filing Date: 10/17/03

Group Art Unit: 2189

Title: SYSTEM AND METHOD FOR RESETTING AND INITIALIZING AN ALAT TO A KNOWN STATE AT POWER ON OR THROUGH MACHINE SPECIFIC STATE

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **09/13/05**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV482711195US, in an envelope addressed to: MS Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: November 10, 2005

Signature: Donna Forbit
Donna Forbit

Respectfully submitted,

David P. Hannum et al.

By Michael J. Fogarty, III
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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Docket No.: 10971353-3
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
David P. Hannum et al.

Application No.: 10/687,907 | Confirmation No.: 1941

Filed: October 17, 2003 | Art Unit: 2189

For: SYSTEM AND METHOD FOR RESETTING AND INITIALIZING AN ALAT TO A KNOWN STATE AT POWER ON OR THROUGH MACHINE SPECIFIC STATE | Examiner: D. Tran

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on September 13, 2005, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter

VI. Grounds of Rejection to be Reviewed on Appeal
VII. Argument
VIII. Claims
IX. Evidence
X. Related Proceedings
Appendix A Claims
Appendix B Evidence
Appendix C Related Proceedings

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Hewlett-Packard Development Company, L.P., a Texas Limited Partnership having its principal place of business in Houston, Texas.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 15 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 4, 5, 14, 15, 20
2. Claims withdrawn from consideration but not canceled: None
3. Claims pending: 1-3, 6-13, 16-19
4. Claims allowed: None
5. Claims rejected: 1-3. 6-13, 16-19

C. Claims On Appeal

The claims on appeal are claims 1-3, 6-13, 16-19

IV. STATUS OF AMENDMENTS

Appellants filed a Response to Non-Final Office Action on March 29, 2005. The Examiner rejected Appellants' arguments in the Final Office Action mailed on June 17, 2005, to which Appellants have filed this Appeal. Appellants did not file an Amendment After Final Rejection. The pending claims are enclosed herein as Appendix A.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following provides a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number and to the drawings by reference characters, as required by 37 C.F.R. § 41.37(c)(1)(v). Each element of the claims is identified by a corresponding reference to the specification and drawings where applicable. Note that the citation to passages in the specification and drawings for each claim element does not imply that the limitations from the specification and drawings should be read into the corresponding claim element.

According to an embodiment of the invention, claim 1 defines a method for preventing matching of prospective entries with table entries stored in a fully associative table (page 10, lines 12-14; figure 2, element 206) comprises the steps of writing illegal values to substantially all of the table entries in the fully associative table (page 9, lines 20-23), and prohibiting the prospective entries from having illegal values under normal program execution conditions (page 8, lines 21-22; page 9, lines 20-23), thereby preventing any matching conditions between the table entries and the prospective entries (page 10, lines 12-14).

According to another embodiment of the invention, claim 3 recites the method of claim 1, where the writing step is initiated by executing a specific machine specific instruction (page 9, lines 2-4).

According to another embodiment of the invention, claim 6 recites the method of claim 1, where the fully associative table is included in a system for finding and validating a most recent advanced load instruction for a given check instruction (page 4, lines 6-10).

According to another embodiment of the invention, claim 9 recites the method of claim 1, comprising the further step of storing register numbers in the fully associative table (page 4, lines 26-28).

According to yet another embodiment of the invention, claim 10 recites the method of claim 1, where the writing step comprises the step of issuing a force update command, thereby causing a plurality of presettable storage elements in the fully associative table to acquire a predetermined illegal value (page 11, lines 1-10).

According to an embodiment of the invention, claim 11 defines a system for preventing matching of prospective entries with table entries stored in a fully associative table (page 10, lines 12-14; figure 2, element 206) comprises means for writing illegal values to substantially all of the table entries in the fully associative table such as, for example, a force update command (page 11, lines 1-4; figure 2, element 203), and means for prohibiting the prospective entries from having illegal values (page 8, lines 21-22; page 9, lines 20-23), thereby preventing any matching conditions between the table entries and the prospective entries (page 10, lines 12-14).

According to another embodiment of the invention, claim 13 recites the system of claim 11, where the writing means is activated by executing a specific machine specific instruction (page 9, lines 2-4).

According to yet another embodiment of the invention, claim 16 recites the system of claim 11, where the fully associative table is included in a system for finding and validating a most recent advanced load instruction for a given check instruction (page 4, lines 6-10).

According to an embodiment of the invention, claim 19 defines a system for disabling matching of prospective entries with entries resident in an fully associative table (page 10, lines 12-14; figure 2, element 206) comprises a plurality of entry locations in the fully

associative table (figure 2, element 206), and a force update command for causing the plurality of entry locations to acquire predetermined illegal bit values not present in prospective entries at ports connected to the fully associative table (page 11, lines 1-4; figure 2, element 203).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1, 2, 7, 8, 10-12, and 17-19 are properly rejected under 35 U.S.C. § 102(b) as being anticipated by Miller et al. (U.S. Patent No. 5,509,528, hereinafter *Miller*).

Whether claims 6, 9, and 16 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over *Miller* in view of Geva (U.S. Patent No. 6,539,541, hereinafter *Geva*).

Whether claims 3 and 13 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over *Miller* in view of Hale et al. (U.S. Patent No. 6,564,317, hereinafter *Hale*).

VII. ARGUMENT

Appellants respectfully traverse the outstanding rejections of the pending claims, and request that the Board reverse the outstanding rejections in light of the remarks contained herein. Below, Appellants argue many of the rejected claims separately. Thus, Appellants respectfully assert that separately argued claims do not stand or fall together, *see* 37 C.F.R. § 41.37(c)(1)(vii).

A. Non-Statutory Double Patenting

Claims 1-3, 6-13, and 16-19 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of U.S. Patent No. 6,823,434. In response, Appellants will file a Terminal Disclaimer that will be in compliance with 37 C.F.R. § 1.321(b), if this rejection still properly stands, upon an indication of allowability on all other matters. Therefore, Appellants respectfully submit that this rejection should be deferred until a later time.

B. Claim Rejections Under 35 U.S.C. § 102 Over *Miller*

Claims 1, 2, 7, 8, 10-12, and 17-19 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Miller*. In order to anticipate a claim under 35 U.S.C. § 102, a single reference must teach each and every element of the claim. *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Appellants respectfully submit that *Miller* fails to teach each and every element of claims 1, 2, 7, 8, 10-12, and 17-19, and respectfully request that this rejection be overturned.

1. Independent Claims 1 and 11, and Dependent Claims 2, 7, 8, 11, 12, 17, and 18

Claim 1 recites, in part, "writing illegal values to substantially all of said table entries in said fully associative table . . . ." Claim 11 recites, in part, "means for writing illegal values to substantially all of said table entries in said fully associative table . . . ." *Miller* does not teach, at least, these elements of claims 1 and 11. Instead, *Miller* teaches that "at initialization . . . all valid status bits are initialized to an invalid state." *Miller*, col. 15, lns. 42-45. Appellants assert that *Miller*'s invalid state is not the same limitation as the claimed illegal values.

The claimed illegal value is defined in the present specification as "a value which a prospective entry would preferably not acquire in a normal course of program execution." Present Specification, page 8, lns. 21-22. On the other hand, *Miller*'s invalid value is a non-current, old or stale value (*Miller*, col. 15, lns. 19-23) which is acquired during the normal course of program execution. *Miller*, col. 3, lns. 13-41. Therefore, because *Miller*'s invalid value is acquired during the normal course of program execution, whereas the claimed illegal value is not, *Miller* does not teach every element of claims 1 and 11.

The Examiner has maintained that "Miller teaches invalid value indicating content of a table entry is not allowed to use (i.e., illegal; e.g., col. 15, lines 17-20 and col. 15, lines 44-46) and the value which a prospective entry would preferably not acquire in a normal course of program execution (e.g., col. 11, lines 55-60; col. 15, lines 35-50)." Final Office Action, page 6. Appellants are aware of the passages cited by the Examiner, and respectfully assert that they do not support the Examiner's contentions. Again, *Miller* explicitly defines an

invalid value as a non-current, old or stale value. *Miller*, col. 15, lns. 19-23. Moreover, it is clear from *Miller*'s disclosure that non-current, old or stale values are acquired during the normal course of program execution. *Miller*, col. 3, lns. 13-41. Therefore, *Miller*'s invalid state is different from the claimed illegal value, which is not acquired during the normal course of program execution. Present Specification, page 8, lns. 21-22.

Therefore, claims 1 and 11 are not anticipated by *Miller*. As such, Appellants respectfully request that the rejection of claims 1 and 11 be overturned.

Dependent claims 2, 7, 8, 12, 17, and 18 depend either from base claims 1 or 11, and thus inherit all of its respective limitations. Therefore, Appellants respectfully submit that claims 2, 7, 8, 12, 17, and 18 are allowable, at least, for the reasons discussed above. Accordingly, Appellants respectfully request that the 35 U.S.C. § 102(b) rejection of claims 2, 7, 8, 12, 17, and 18 be overturned.

2. Dependent Claim 10

Claim 10 recites, in part, "issuing a force update command." *Miller* does not teach the claimed force update command. At the first passage cited by the Examiner, *Miller* simply teaches a system initialization procedure. *Miller*, col. 15, lns. 35-50. *Miller*'s initialization procedure does not include a force update command for causing a plurality of entry locations to acquire predetermined illegal bit values, as required by claim 10. At the second passage cited by Examiner, *Miller* teaches a snoop operation for identifying an invalid entry (i.e., an entry containing a non-current, stale or old value) and for setting a flag to indicate that the entry is invalid. *Miller*, col. 3, lns. 21-24; col. 16, lns. 11-15. Appellants assert that that a force update command for causing a plurality of entry locations to acquire predetermined illegal bit values, as required by claim 10, is not the same limitation as *Miller*'s system initialization procedure, nor is it the same as *Miller*'s operation for identifying an invalid table entry and setting an invalid entry flag. Accordingly, *Miller* does not anticipate claim 10 and Appellants respectfully request that the 35 U.S.C. § 102(b) rejection of record be overturned.

3. Independent Claim 19

Claim 19 recites, in part, "a force update command for causing said plurality of entry locations to acquire predetermined illegal bit values not present in prospective entries at ports connected to said fully associative table." First, as noted above, *Miller* does not teach, at least, the claimed illegal values. Second, as also noted above, *Miller* does not teach the claimed force update command. Accordingly, *Miller* does not anticipate claim 19 and Appellants respectfully request that the 35 U.S.C. § 102(b) rejection of record be overturned

C. Claim Rejections Under 35 U.S.C. § 103 Over *Miller* in View of *Geva*

Claims 6, 9, and 16 are rejected under 35 U.S.C. § 103 as being unpatentable over *Miller* in view of *Geva*. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Without conceding the second criteria, Appellants assert that the rejection does not satisfy the third criteria and respectfully request that this rejection be overturned.

1. Dependent Claims 6 and 16

Claim 1 recites, in part, "writing illegal values to substantially all of said table entries in said fully associative table . . . ." Claim 11 recites, in part, "means for writing illegal values to substantially all of said table entries in said fully associative table . . . ." As noted above, *Miller* does not teach or suggest, at least, these elements of claims 1 and 11. Appellants assert that *Geva* does not teach or suggest this limitation either, and notes that the Examiner has not relied upon *Geva* as such. Hence, the combination of *Miller* and *Geva* does not teach or suggest every limitation of claims 1 and 11. Claims 6 and 16 depend from base claims 1 and 11, respectively, thus inheriting all of their respective limitations. Therefore, the combination of *Miller* and *Geva* does not teach or suggest every limitation of claims 6 and 16. Accordingly, Appellants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 6 and 16 be overturned.

In addition, claim 6 and 16 each recite, in part, "a system for finding and validating a most recent advanced load instruction for a given check instruction." The Examiner relies on *Geva* as providing "a most recent advanced load instruction for a given check instruction (e.g., col. 14, lines 15-65)." Final Office Action, page 5. However, this is not the same limitation as the system for finding and validating the advanced load instruction, as required by claims 6 and 16. Appellants cannot find any other section of *Miller* or *Geva* that teaches or suggests the claimed limitation. Accordingly, Appellants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 6 and 16 be overturned.

Finally, claims 6 and 16 are allowable because there is no suggestion or motivation to combine the teachings of *Miller* and *Geva*. The Examiner contends that:

> [i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Geva into the system of Miller because it would allow handling advanced loads in a cache system; thereby increasing the performance and speed processing of the system. Final Office Action, page 5.

Appellants point out that *Miller* discloses a method of handling invalid data in a cache memory system, whereas *Geva* teaches a method for compiling loop instructions. *See Miller*, col. 1, lns. 8-12; *Geva*, col. 4, lns. 25-38. There is no suggestion either in the references themselves or in the knowledge generally available to one of ordinary skill in the art that *Miller*'s method for handling invalid data in a memory is combinable with, or would benefit from, *Geva*'s method of compiling a loop instruction. Accordingly, Appellants respectfully assert that, for the above reasons, claims 6 and 16 are patentable over the 35 U.S.C. § 103(a) rejection of record.

2. Dependent Claim 9

Claim 1 recites, in part, "writing illegal values to substantially all of said table entries in said fully associative table . . . ." As noted above, *Miller* does not teach or suggest, at least, these elements of claim 1. Appellants assert that *Geva* does not teach or suggest this limitation either, and notes that the Examiner has not relied upon *Geva* as such. Hence, the combination of *Miller* and *Geva* does not teach or suggest every limitation of claim 1. Claim 9 depends from base claim 1, thus inheriting all of its limitations. Therefore, the combination

of *Miller* and *Geva* does not teach or suggest every limitation of claim 9. Accordingly, Appellants respectfully request that the 35 U.S.C. § 103(a) rejection of claim 9 be overturned.

In addition, claim 9 is allowable because there is no suggestion or motivation to combine the teachings of *Miller* and *Geva*. The Examiner contends that:

> [i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Geva into the system of Miller because it would allow handling advanced loads in a cache system; thereby increasing the performance and speed processing of the system. Final Office Action, page 5.

Appellants point out that *Miller* discloses a method of handling invalid data in a cache memory system, whereas *Geva* teaches a method for compiling loop instructions. *See Miller*, col. 1, lns. 8-12; *Geva*, col. 4, lns. 25-38. There is no suggestion either in the references themselves or in the knowledge generally available to one of ordinary skill in the art that *Miller*'s method for handling invalid data in a memory is combinable with, or would benefit from, *Geva*'s method of compiling a loop instruction. Accordingly, Appellants respectfully assert that, for the above reasons, claim 9 is patentable over the 35 U.S.C. § 103(a) rejection of record.

D. Claim Rejections Under 35 U.S.C. § 103 Over *Miller* in View of *Hale*

Claims 3 and 13 are rejected under 35 U.S.C. § 103 as being unpatentable over *Miller* in view of *Hale*. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Without conceding the first or second criteria, Appellants assert that the rejection does not satisfy the third criteria and respectfully request that this rejection be overturned.

1. Dependent Claims 3 and 13

Claim 1 recites, in part, "writing illegal values to substantially all of said table entries in said fully associative table . . . ." Claim 11 defines, in part, "means for writing illegal values to substantially all of said table entries in said fully associative table . . . ." As noted above, *Miller* does not teach or suggest, at least, these elements of claims 1 and 11. Appellants assert that *Hale* does not teach or suggest this limitation either, and notes that the Examiner has not relied upon *Hale* as such. Hence, the combination of *Miller* and *Hale* does not teach or suggest every limitation of claims 1 and 11. Claims 3 and 13 depend from base claims 1 and 11, respectively, and thus inherit all of their respective limitations. Therefore, the combination of *Miller* and *Hale* does not teach or suggest every limitation of claims 3 and 13. Accordingly, Appellants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 3 and 13 be overturned.

In addition, claims 3 and 13 are allowable because there is no suggestion or motivation to combine the teachings of *Miller* and *Hale*. The Examiner contends that:

> [i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Hale into the system of Miller because it would allow a secure boot process when performing initialization of a computer system upon power up or system reset. Final Office Action, page 6.

Appellants point out that *Miller* discloses a method of handling invalid data in a cache memory system, whereas *Hale* teaches a method for securing computer firmware during initialization. *See Miller*, col. 1, lns. 8-12; *Hale*, Abstract. There is no suggestion either in the references themselves or in the knowledge generally available to one of ordinary skill in the art that *Miller*'s method for handling invalid data in a memory is combinable with, or would benefit from, *Hale*'s method of initializing a computer system.

Moreover, the language of the Examiner's proposed motivation is merely a statement that the references can be combined and does not state any desirability for making the combination. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). Neither the prior art nor the

knowledge available to a person of ordinary skill in the art suggest the desirability of the combination. Accordingly, Appellants respectfully assert that, for the above reasons, claims 3 and 13 are patentable over the 35 U.S.C. § 103(a) rejection of record.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Dated: November 10, 2005

Respectfully submitted,

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV482711195US, in an envelope addressed to: MS Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: November 10, 2005

Signature: Donna Forbit
Donna Forbit

By Michael J. Fogarty, III
Michael J. Fogarty, III
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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/687,907

1. (Original) A method for preventing matching of prospective entries with table entries stored in a fully associative table, the method comprising the steps of:

writing illegal values to substantially all of said table entries in said fully associative table; and

prohibiting said prospective entries from having said illegal values under normal program execution conditions, thereby preventing any matching conditions between said table entries and said prospective entries.

2. (Original) The method of claim 1 wherein said writing step is performed during power up of a system.

3. (Original) The method of claim 1 wherein said writing step is initiated by executing a specific machine specific instruction.

4. (Canceled)

5. (Canceled)

6. (Original) The method of claim 1 wherein said fully associative table is included in a system for finding and validating a most recent advanced load instruction for a given check instruction.

7. (Original) The method of claim 1 comprising the further step of:

updating entries in a fully associative table employing a pointer to indicate a first table location containing an invalid entry.

8. (Original) The method of claim 1 comprising the further step of:

storing memory addresses in said fully associative table.

9. (Original) The method of claim 1 comprising the further step of:

storing register numbers in said fully associative table.

10. (Original) The method of claim 1 wherein said writing step comprises the step of:

issuing a force update command, thereby causing a plurality of presettable storage elements in said fully associative table to acquire a predetermined illegal value.

11. (Original) A system for preventing matching of prospective entries with table entries stored in a fully associative table, the system comprising:

means for writing illegal values to substantially all of said table entries in said fully associative table; and

means for prohibiting said prospective entries from having said illegal values, thereby preventing any matching conditions between said table entries and said prospective entries.

12. (Original) The system of claim 11 wherein said writing means operates during power up of a system.

13. (Original) The system of claim 11 wherein said writing means is activated by executing a specific machine specific instruction.

14. (Canceled)

15. (Canceled)

16. (Original) The system of claim 11 wherein said fully associative table is included in a system for finding and validating a most recent advanced load instruction for a given check instruction.

17. (Original) The system of claim 11 further comprising:

means for updating entries in a fully associative table employing a pointer to indicate a first table location containing an invalid entry.

18. (Original) The system of claim 11 further comprising:

means for storing memory addresses in said fully associative table.

19. (Previously Presented) A system for disabling matching of prospective entries with entries resident in an fully associative table, the system comprising:

a plurality of entry locations in said fully associative table; and

a force update command for causing said plurality of entry locations to acquire predetermined illegal bit values not present in prospective entries at ports connected to said fully associative table.

20. (Canceled)